FINISAR

DSFP MIS Proposal to DSFP MSA

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Status of DSFP MIS Proposals

Slide content removed on 9/6/18 to enable public posting

Finisar DSFP MIS Proposal Timeline

- Finisar DSFP MIS recommendation first sent out to the full DSFP MSA on 24 Feb. 2018:
  - Use the Advisors module level state machine
  - Drop data path state machine
  - Use the Advisors memory map
  - Drop bank control so there is only a paged memory map
  - Write the changes as a separate DSFP MIS spec. referencing Advisors
- We continue with that recommendation, plus:
  - Given identical HW I/O structure between OSFP and DSFP, we recommend same HW I/O pin definition.

56G PAM4 (Host Side) Form Factor Overview

Module	Lane Count	Hardware Management Interface	Management MSA
SFP56	1	Mod_ABS, Tx_Disable, Rx_LOS, Tx_Fault, RS0, RS1, SDA, SCL	SFF-8472 (Rev. 12.2)
SFP-DD (Rev. 1.1)	2	TxFault, TxFaultDD, TxDisable, TxDisableDD, Mod_ABS, RS0, RS0DD, RS1, RS1DD, LOS, LOSDD, IntL, InitMode, SDA, SCL	SFP-DD Rev 1.1 (HW Spec) MIS is pending (Tom P)
QSFP56	4	ModselL, ResetL, ModPrsL, IntL, LPMode, SDA, SCL	SFF-8636 Rev 2.7 (Rev. 2.9 exists like CMIS, Intel, Tom P, Barry Olawsky)
QSFP-DD	8	ModselL, ResetL, ModPrsL, IntL, InitMode, SDA, SCL	CMIS 2.7
OSFP	8	LPWn/PRSn, INT/RSTn, SDA, SCL	CMIS 2.7 + Addendum
DSFP	2	LPWn/PRSn, INT/RSTn, SDA, SCL	CMIS 2.7 + Addendum
CFP8	8	CFP MSA + CFP8 HW spec, MDIO	CFP MSA MIS Ver. 2.6

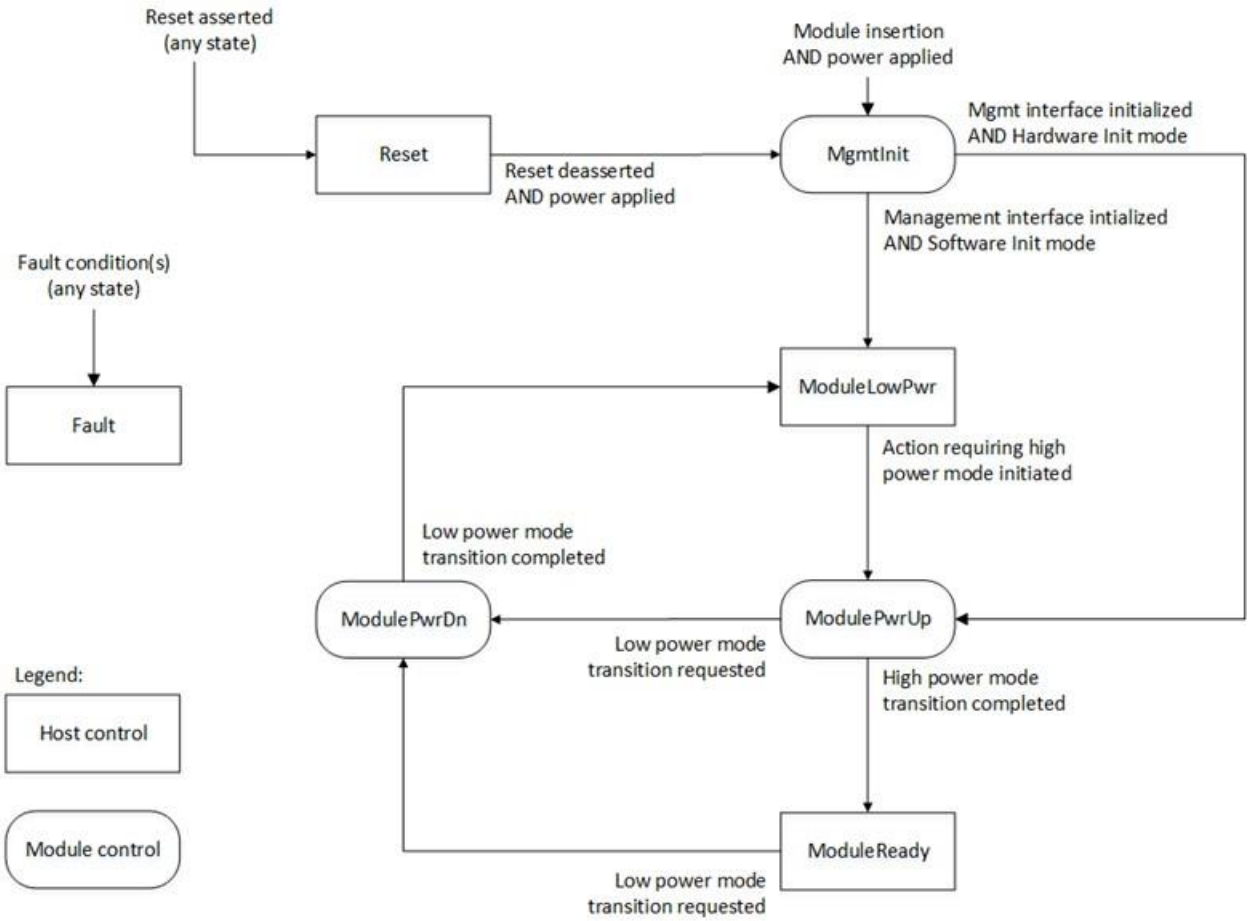
QSFP-DD and OSFP HW I/O Pin Equivalents

QSFP-DD	OSFP & DSFP	Comment
ModselL	n/a	No OSFP equivalent
ResetL	RSTn	same
ModPrsL	PRSn	same
IntL	INT	same
InitMode	LPWn	Different functions between OPSF and QSFP-DD
SDA	SDA	same
SCL	SCL	same

DSFP Management Interface Highlights

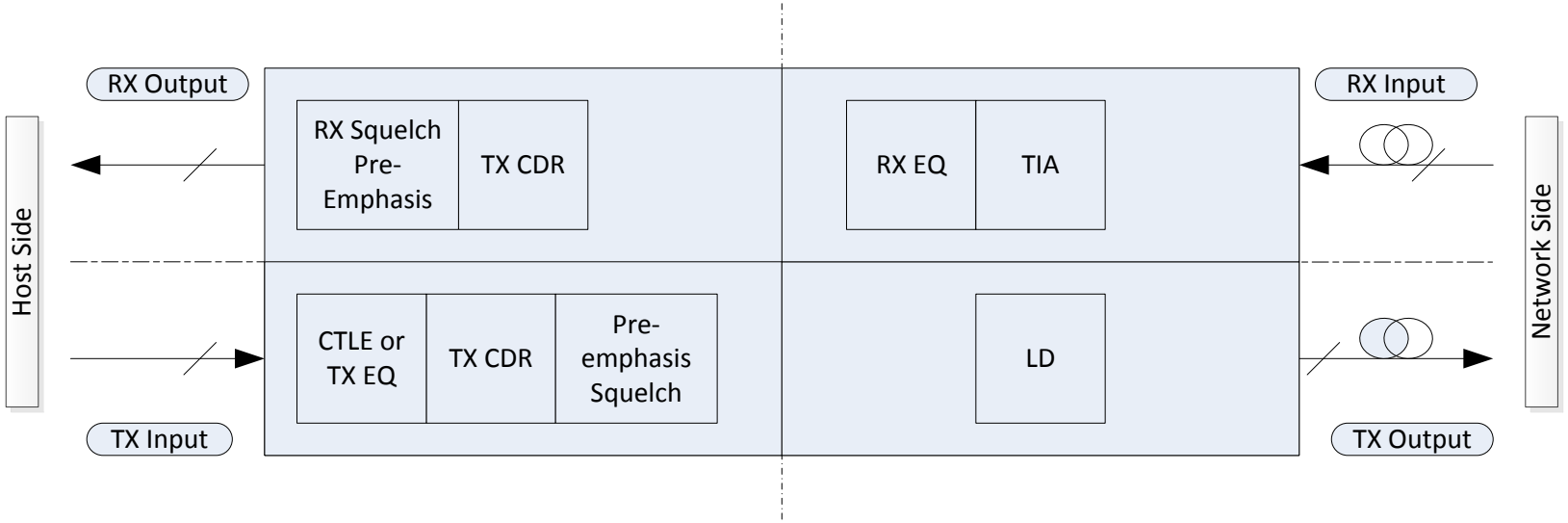
- Present both module and all lane level diagnostics and control to host due to its nature of being physical level device
- Adopt Module Level State Machine from CMIS, which sufficiently describes the module and lane behavior
- Omits Data Path concept in module and leave Data Path State Machine managed by host, for the simplicity of module
- Keep the Lane State concept specified by CMIS
- For simplicity, DSFP memory map omits “Bank” specifications but remains fully compatibility by leaving “Bank Select” byte under reserve

DSFP Proposals – Module State Machine

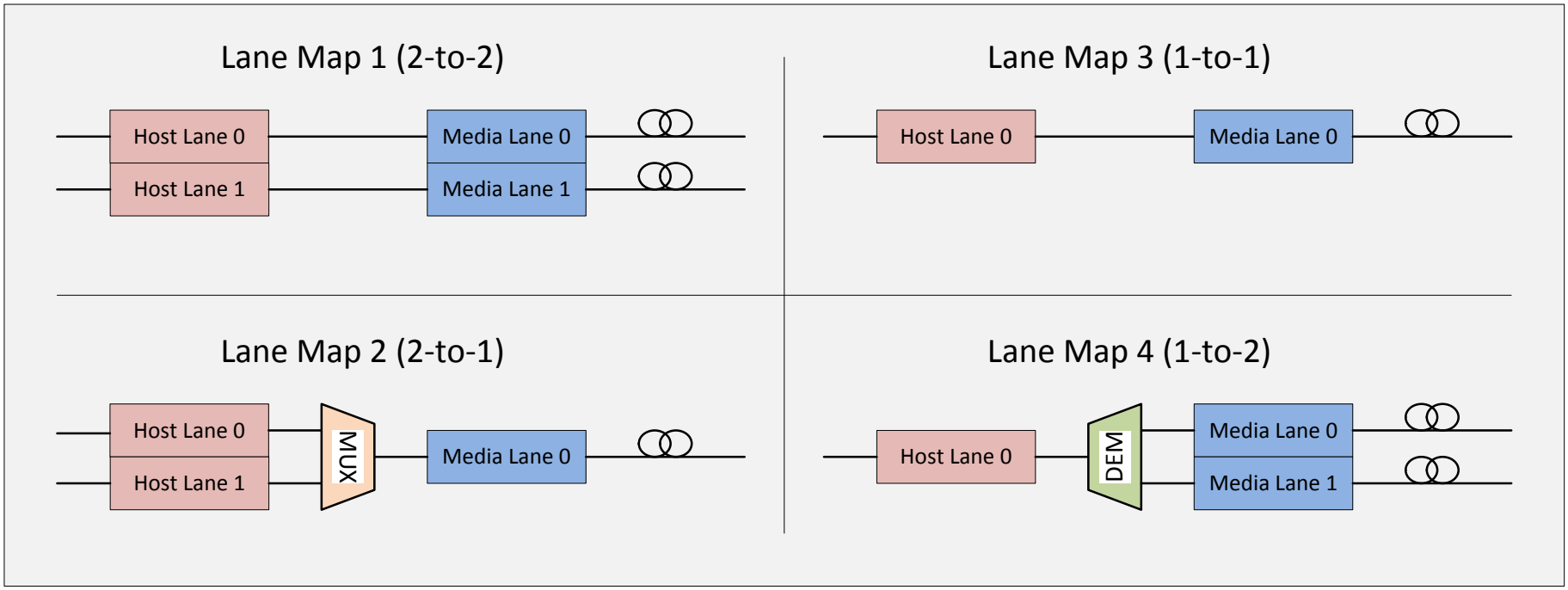


- DSFP adopts CMIS module level state machine
- DSFP omits DataPath state machine for simplicity
- Advertise timing for each transient state
- Host specifies data path as a logical concept by configurating lanes either based on presets (Staged) or dynamically in module Low Power state

DSFP Module Block Diagram

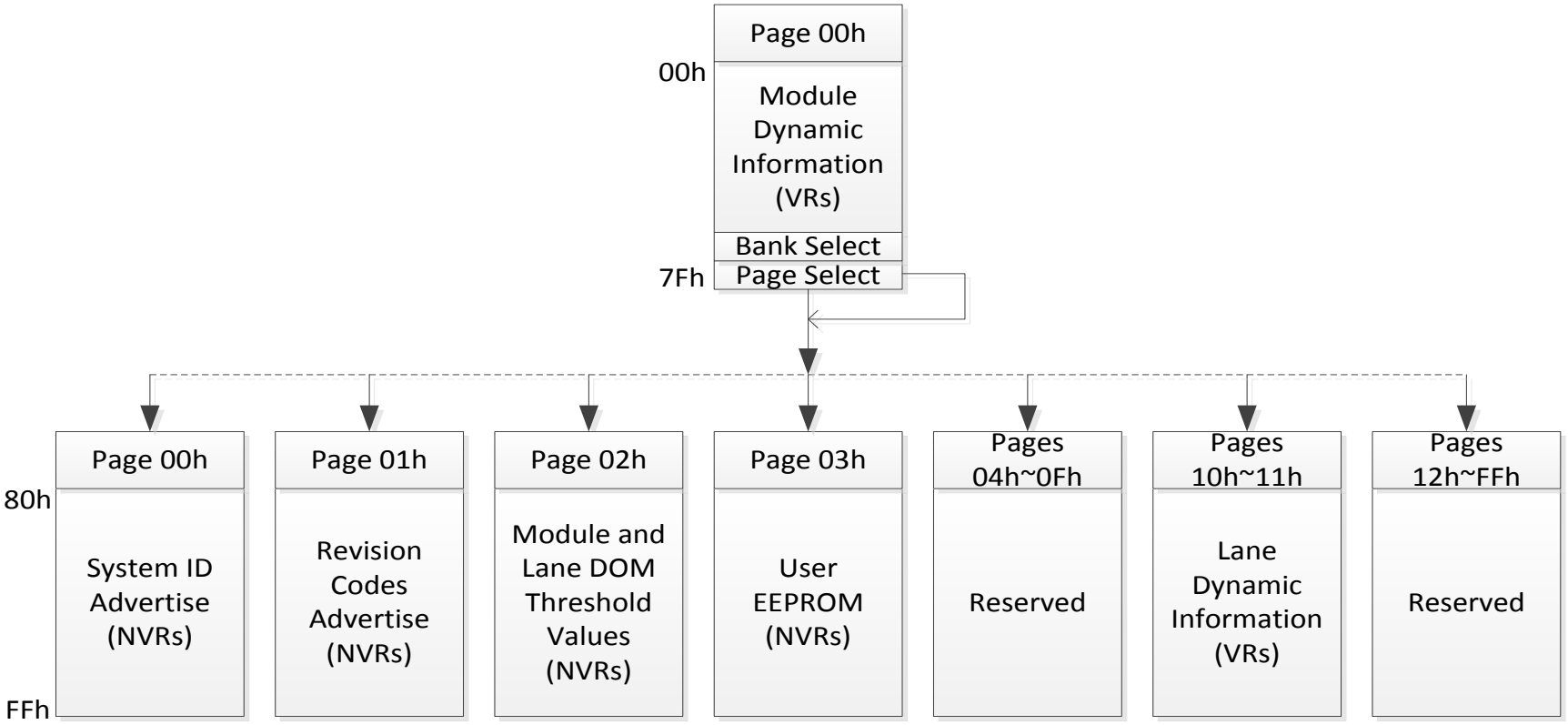


DSFP Lane Mapping and Configuration



- Only limited number of lane mapping possible
- One module may only implement one lane mapping
- Assign a lane mapping with a numerical code
- Vendor advertises a module with a lane map number
- Data path configuration is limited by physical lane mapping of a module
- TX-RX symmetry is assumed in above drawings

Memory Map

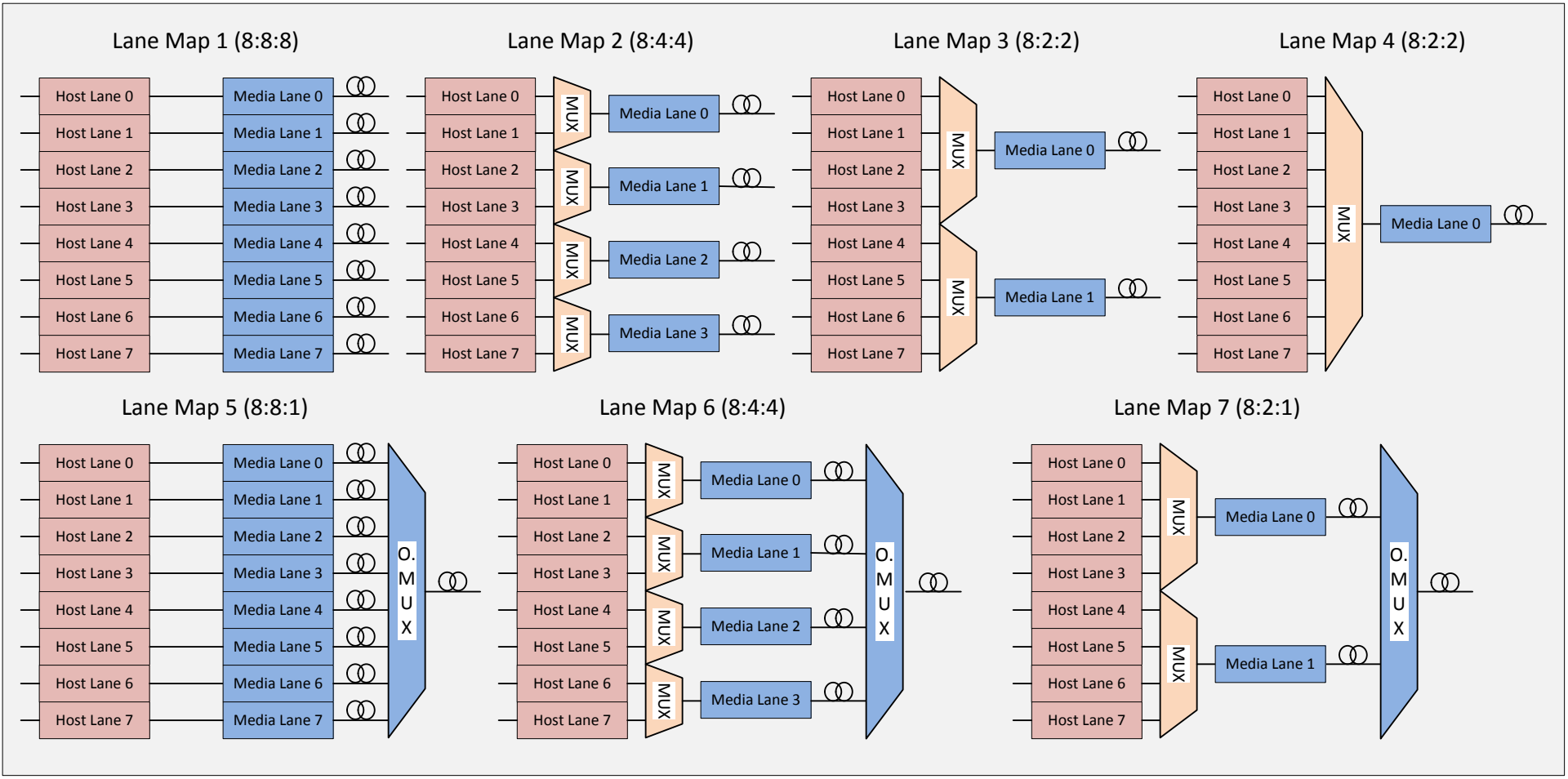


- Need (max) 4x128 Bytes of NVR (EEPROM), 3x128 bytes of VR (RAM)
- Bank select byte is reserved for CMIS compatibility
- Similar content to CMIS with compatible changes

Memory Map Details

- DSFP Identification is per SFF-8024, currently
  - 18h is assigned to QSFP-DD
  - 19h and 1Ah are likely used by OSFP and SFP-DD
  - So 1Bh is a good candidate (TBD)
- Page 10h Byte 128 will be changed to “Lane Power Control” from “Datapath Lane Power Control”.
- Page 11h Bytes 128~131 will be changed to “Lane State Indicators” from “Datapath State indicators”.

Appendix: Lane Mapping and Configuration for OSFP



- MIS can code each lane map with a number
- 7 typical cases listed above, but new lane map can always be added to the code as technology moves forward
- Question: is a module capable supporting more than one lane map?